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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,252	06/28/2001	Atila Alvandpour	42390.P11944	9190

7590 10/11/2002

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EXAMINER
CHANG, DANIEL D

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,252	ALVANDPOUR ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/24/2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Drawings

The drawings are objected to because a circle is missing at the gate of 208 in figure 2. The informal drawing shows the circle but the formal drawing does not show the circle. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 11 and 13 are objected to because of the following informalities: on line 2, the wording, such as --coupled-- should be inserted to particularly point out and distinctly claim the subject matter. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 8-11, 13, 15, 18, and 21-24 are rejected under 35 U.S.C. 102(a) as being anticipated by the Applicant's Admitted Prior Art (Fig. 1).

Regarding claims 1 and 24, the Applicant's Admitted Prior Art discloses, in fig. 1, a dynamic circuit having an evaluation phase, the dynamic circuit comprising:

a node (11);

a power rail (Power Supply);

at least one nMOSFET (102) to conditionally pull the node LOW during the evaluation phase; and

a conditional keeper comprising:

a NAND gate (112, 114) having a first input port (gate of 112) connected to the node (via 106) and an output port (drain of 114); and

a first pMOSFET (108) having a gate connected to the output port of the NAND gate (via 106) and having a drain connected to the node.

Regarding claim 8, the Applicant's Admitted Prior Art discloses, in fig. 1, a dynamic circuit having a normal operating condition and a burn-in condition, the dynamic circuit comprising:

a node (110) having a voltage;

a network (102) comprising at least one transistor to conditionally pull the node LOW;

a logic gate (112, 114) having a first input port (gate of 112) responsive to the node voltage (via 106), a second input port (BI-ACTIVE), and an output port (drain of 114) having a voltage;

a first transistor (108) responsive to the output port voltage of the logic gate (via 106), and coupled to the node; and

wherein the first transistor and the logic gate provide a keeper function to the node if and only if the second input port (BI-ACTIVE) of the logic gate is at a voltage indicative of the dynamic circuit being in the burn-in condition.

Regarding claims 9 and 22, the Applicant's Admitted Prior Art discloses, in fig. 1, that the first transistor (108) is a pMOSFET having a gate connected to the output port of the logic gate (via 106) and a drain connected to the node.

Regarding claims 10 and 23, the Applicant's Admitted Prior Art discloses, in fig. 1, that the logic gate is a NAND gate (112, 114).

Regarding claims 11 and 13, the Applicant's Admitted Prior Art discloses, in fig. 1, a second transistor (112) coupled (via 114) to the node; and

an inverter (106) coupled to the second transistor and the node, so that the combination of the second transistor and the inverter provide a keeper function to the node.

Regarding claims 15, 18, 21, the Applicant's Admitted Prior Art discloses, in fig. 1, that the power rail connected to the source of the first pMOSFET (108).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-7, 12, 14, 16, 17, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (Fig. 1).

The teachings of the Applicant's Admitted Prior Art have been discussed above.

Regarding claims 3, 4, 5 and 17, the Applicant's Admitted Prior Art teaches that the first transistor (108) is responsive to the output port voltage of the NAND gate (via 106) to pull the

node **HIGH** only if the second input port (BI-ACTIVE) of the NAND gate is **LOW** but does not disclose that the first transistor (108) pulls the node **HIGH** when the second input port of the NAND gate is **HIGH**.

However, it is well known in the art that an inverter inverts a signal at its output respect to its input. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have provided a dynamic circuit of the Applicant's Admitted Prior Art with a well known inverter at the second input port (BI-ACTIVE) to proved an inverted signal. It is an obvious matter of design choice.

Regarding claims 6 and 19, the Applicant's Admitted Prior Art discloses, in fig. 1, an inverter (106) coupled to the inverter (106) and the node (via 114) to provide a keeper function.

Regarding claims 2, 7, 12, 14, 16, and 20, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to size the first pMOSFET larger than the second pMOSFET to the modified circuit as discussed above because the first pMOSFET inhibits the detrimental effects of charge loss that are expected to occur under more severe conditions and the second pMOSFET minimizes the capacitance it contributes to precharge the node.

Response to Arguments

Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

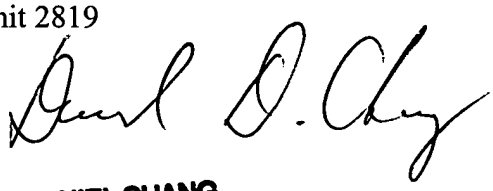
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Daniel D. Chang
Primary Examiner
Art Unit 2819



DANIEL CHANG
PRIMARY EXAMINER

DC
October 1, 2002